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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,754	08/17/2001	Emil Kamieniecki	QCS-001DV3	5384
21323	7590	07/13/2004	EXAMINER	
TESTA, HURWITZ & THIBEAULT, LLP HIGH STREET TOWER 125 HIGH STREET BOSTON, MA 02110			HOLLINGTON, JERMELE M	
			ART UNIT	PAPER NUMBER
			2829	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/932,754

Applicant(s)

KAMIENIECKI ET AL.

Examiner

Jermele M. Hollington

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 May 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 53-57 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 53-57 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 53 is objected to because of the following informalities: claim 53 recites: “a conveying apparatus conveying said wafer adjacent said voltage sensor of the head assembly under the head assembly during processing.” The claim language is confusing to the examiner. It is not clear where the wafer is conveying from and what location it is conveying to. From the claim language, it appears it is conveying from the voltage sensor to the head assembly. However, other claim limitations in claim 53 describe that the voltage sensor is already part of the head assembly and therefore it is not conveying from the voltage sensor to the head assembly. Therefore, the examiner is taking a position that the wafer is conveying from outside of the head assembly into the head assembly near the vicinity of the voltage sensor. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

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the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 53-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamieniecki et al (5091691) in view of Yoshino et al (5708365).

Regarding claim 53, Kamieniecki discloses [see Fig. 17] an apparatus for making surface photovoltage measurements of a semiconductor comprising a sealed chamber (represented as enclosure 197) [see column 12 lines 15-19] for processing the semiconductor wafer (represented as specimen 11) [see column 4 lines 34-37 and column 6 lines 32-36] having a first surface and a second surface [see Fig. 17] and a head assembly (represented as arrangement 191) having a modulated light source (43) exposing [via glass plate 201] at least a portion of the semiconductor wafer (11) to light having a wavelength and modulated at a frequency [see column 7 lines 29-35 and lines 49-62 and column 12 lines 39-42] and a surface photovoltage sensor (represented as reference electrode assembly 199) comprising a plurality of electrodes (transparent plate 201, edge pick up areas 205, 207 and 209 and central pickup area 203) positioned adjacent to the first surface [see Fig. 17] to detect a surface photovoltage [see Abstract lines 6-8] induced at the first surface of the semiconductor wafer (11) in response to the light [via light source 43] without contacting the wafer (11) [see column 12 lines 39-50], the plurality of electrodes (201, 203, 205, 207 and 209) sufficient for detecting the surface photo-voltage on the first surface and the surface photo-voltage sensor (199) of head assembly (191) located within the sealed chamber (197). However, Kamieniecki et al do not disclose a conveying apparatus as claimed. Yoshino et al disclose [see Fig. 2] a semiconductor wafer fabrication system comprising a head assembly

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[shown in Fig. 2] comprising a modulated light source (Halogen Light Source) exposing at least a portion of a semiconductor wafer (Silicon Wafer) to light (white light), a surface photo voltage sensor (SPV Transducer) comprising a plurality of electrodes (SPV signal) positioned adjacent a first surface [top surface] to detect a surface photo voltage induced at the first surface [top surface] of the semiconductor wafer (Silicon Wafer) and a conveying apparatus (combination of Wafer Chuck, Moving Stage and Stepping Motor Control Drive) conveying the wafer (Silicon Wafer) adjacent the voltage sensor (SPV Transducer) of the head assembly [shown in Fig. 2] under head assembly during processing [measuring diffusion length of the wafer]. Further, Yoshino et al teach that the addition of conveying apparatus is advantageous because it moves the wafer around so that the SPV sensor (transducer) is able to evaluate the dielectric breakdown of an oxide layer on the wafer. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Kamieniecki et al by adding a conveying apparatus as taught by Yoshino et al in order to move the wafer around so that the SPV sensor (transducer) is able to evaluate the dielectric breakdown of the wafer during fabrication.

Regarding claims 54-56, Kamieniecki discloses the sealed chamber (197) as a reduced pressure chamber, a chemically reactive gas chamber or an inert environment chamber [see column 12 lines 15-16 and column 13 lines 42-46].

Regarding claim 57, Kamieniecki discloses [see fig. 17] the head assembly (191) is entirely located within the sealed chamber (197).

Conclusion

5. Applicant's arguments filed May 14, 2004 have been fully considered but they are not persuasive.

The applicants' state: *"In both cited references, the wafer is loaded beneath the head and measured individually in a manner suitable only for low volume wafer measurements. The conveying apparatus as recited in claims 53-57 of the present invention makes Applicants' invention suitable for high volume production line measurements of wafer characteristics taken during processing..."* Further, the applicants state: *"Yoshino does not teach moving the moving stage to move allow in-process high volume wafer measurement."*

In response to the above statements, the examiner will like to remind the applicants "Limitations appearing in the specification but not recited in the claim are not read into the claim" [see *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969)]. Therefore, it is noted that the features upon which applicant relies (i.e., suitable for high volume production line measurements) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The applicants argues: *"In other words, adjusting the moving stage to move the wafer away from the SPV Transducer in order to remove that wafer and physically replace it with another wafer is still an interrupting of the process flow, and cannot occur in a processing environment. The present invention conveys the wafers under the head assembly during processing without interrupting process flow."*

In response to the above statement, base on the claim limitations presented in claim 53, the present invention does have interrupting process flow. The claim states: "A semiconductor

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wafer fabrication system...” Also it states: “... a conveying apparatus conveying said wafer...”

Base on the above claim limitations, there is only a (one) wafer that is being conveyed during the fabrication system. As a result, if other wafers are being conveyed into the head assembly the process have to be interrupted to remove one wafer and to process another wafer.

The applicants argue: *“However, neither Kamienieki nor Yoshino teach an arrangement that permits the mapping of the wafer during wafer processing.”*

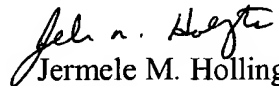
In response to the above statements, the examiner will like to remind the applicants “Limitations appearing in the specification but not recited in the claim are not read into the claim” [see *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969)]. Therefore, it is noted that the features upon which applicant relies (i.e., mapping of the wafer during wafer processing) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Kamand Cuneo can be reached on (517) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Jermele M. Hollington
Examiner
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JMH
July 8, 2004